Remarks:

Reconsideration of the above referenced application in view of the enclosed amendment and remarks is requested. Claims 1, 3, 7-9, and 16 are amended. Claims 23-28 are added to recite an additional embodiment of the invention. Claims 1, 3-5 and 7-28 remain in the application.

ARGUMENT

Claims 1, 3, 4, 9, 10, 11, 13, 16, 17, 18 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over USPN 6,397,242 to Devine (hereinafter "Devine") in view of "*The Technology Behind Crusoe Processors*" by Alexander Klaiber (hereinafter "Klaiber) and further in view of view of USPN 6,496,847 to Bugnion et al. (hereinafter "Bugnion et al."). This rejection is respectfully traversed and Claims 1, 3, 4, 9, 10, 11, 13, 16, 17, 18 and 20 are believed allowable as amended based on the following discussion.

The Examiner asserts that Bugnion et al. teach an operating system executing on the host machine supporting a full platform simulator. This assertion is not accurate, especially as applied to Applicants description and claimed invention. Bugnion et al. teach a conventional system model for incorporating an emulator to emulate actual device and resource requests. In fact, Bugnion et al. refer to the emulator as a "device emulator 200" at Col. 6, line 59 to more clearly refine what is meant in their description. Bugnion et al. teach that a user executing applications in a VM may access hardware devices via an emulator communicating with the host OS. The emulator uses the services of the host OS 240 to manage system resources. (Col. 7, lines 3-5). This enables the VM to be generalized and unaware of the hardware types.

In contrast, Applicants' claimed invention is for simulating a target CPU, for instance an instruction set architecture (ISA), in the virtual machine. As described in the specification at least on page 4, "the simulated OS 151 code runs in the VM 15." Further, simulated instructions that access CPU system state, e.g., control registers, are intercepted and simulated in the VMM and translated so that when the VM executes the instructions, they are simulated in the full platform simulator in the host environment. Claims 1, 9 and 16 are amended to specifically

recite that *the simulator to execute the translated code that represents simulated operating system code to be executed on the virtual machine*. Bugnion et al. do not teach or suggest that a target CPU is to be simulated in the VM. Instead Bugnion et al. teach that the VM runs several applications 230 in the VM (Fig. 2). Bugnion et al. further teach that the applications in the VM require device access which is emulated as a bridge between the VM and the hardware. Bugnion et al. do not teach or suggest that operating system codes are simulated with translated code and executed in a full platform simulator to allow a target CPU to be simulated in a VM. Thus, combining the device emulator of Bugnion et al. with the teachings of Devine and Klaiber will not result in Applicants' claimed invention. At no time do the cited references, either alone or in combination, teach the simulation of simulated OS code in the host machine.

Moreover, the Examiner's assertion that Bugnion et al. teach a full platform simulator is inaccurate, as mentioned above. Bugnion et al. imply that the emulator is merely a device emulator in Col. 6, line 59, and therefore teaches away from the concept of a full platform simulator. Thus, Claims 1, 3, 4, 9, 10, 11, 13, 16, 17, 18 and 20 are believed allowable as amended.

Claims 5, 12 and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Devine and Klaiber in view of "*Running multiple operating systems concurrently on an IA32 PC using virtualization techniques*" by Kevin Lawton (hereinafter "Lawton").

Claims 7, 8, 14, 15, 21 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Devine and Klaiber in view of "*Operating systems internals and design principles*" by William Stallings (hereinafter "Stallings").

These rejections are respectfully traversed and Claims 5, 7, 8, 12, 14, 15, 19, 21 and 22 are believed allowable as amended based on the foregoing and following discussion.

Independent Claims 1, 9 and 16 are amended to require that *an operating system executing on the host machine also supports a full platform simulator that includes device models, the simulator to execute the translated code that represents simulated operating system code to be executed on the virtual machine*. The Examiner contends in of the Office Action that Bugnion et al. supports a full platform simulator. This assertion is in error, as discussed above. Bugnion et al. shows device emulators and I/O emulation modules for use with a virtual machine monitor (VMM). The prior art Figure 2 as described by Bugnion et al. shows another

architecture for a VM running user applications to access hardware resources via a device emulator. This is in contrast to Applicants' claimed invention. Figure 1 shows that the software simulator (SoftSDV) is part of the Host Environment 101. The VMM is shown as part of the Direct Execution Environment 102. Applicants' claims require that the operating system on the host machine (not the VMM) provide the full platform simulator for simulating simulated operating system code. This enables instruction set architectures (ISAs) to be simulated using VMs. The full platform simulator simulates the full PC hardware platform, as described in the specification. This simulation of the full platform to execute simulate OS code is not taught or suggested by any of the cited references. Further, application of Bugnion et al. to Devine and Klaiber or the other references will not result in a virtualized platform that enables ISA simulation as does Applicants' claimed invention.

Thus, all claims remaining in the application are now allowable.

CONCLUSION

In view of the foregoing, Claims 1, 3-5 and 7-28 are all in condition for allowance. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (703) 633-6845. Early issuance of Notice of Allowance is respectfully requested. Please charge any shortage of fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such account.

Respectfully submitted,

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s/ Joni D. Stutman-Horn /

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